IN THE CLAIMS

1. (Currently Amended) A semiconductor structure for storing charges, comprising:

an insulator layer having a first compound that includes substances; and

a single conductive layer having a second compound that includes a first substance and a second substance, wherein the single conductive layer also includes a trace amount of the first substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer.

D1

2. (Original) The semiconductor structure of claim 1, wherein the first compound includes ditantalum pentaoxide.

3. (Original) The semiconductor structure of claim 1, wherein the first substance includes ruthenium atoms.

D2

4. (Original) The semiconductor structure of claim 1, wherein the second substance includes oxygen atoms.

5. (Original) The semiconductor structure of claim 1, wherein the second compound includes RuOx, wherein x is indicative of a desired number of atoms.

6. (Currently Amended) A semiconductor structure for storing charges, comprising:

an insulator layer; and

a single conductive layer having a compound formed from a first substance and a second substance, wherein the single conductive layer also includes a trace amount of the first substance, wherein the morphology of the semiconductor structure remains stable when the trace amount of the first substance is oxidized during crystallization of the insulator layer.

D3

7. (Original) The semiconductor structure of claim 6, wherein the compound includes RuOx, wherein x is indicative of a desired number of atoms.

D4

[redacted]

8. (Original) The semiconductor structure of claim 6, wherein the first substance includes ruthenium.

D4

9. (Original) The semiconductor structure of claim 6, wherein the second substance includes oxygen.

10. (Original) The semiconductor structure of claim 6, wherein the insulator layer includes ditantalum pentaoxide.

D5

11. (Currently Amended) A semiconductor structure for storing charges, comprising:
an insulator layer having a permittivity value greater than about 25; and
a single conductive layer having a compound and a substance, wherein the compound remains stable when the insulator layer is crystallized at a high temperature so as to decrease the charge leakage of the insulator layer.

12. (Original) The semiconductor structure of claim 11, wherein the insulator layer includes ditantalum pentaoxide.

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13. (Original) The semiconductor structure of claim 11, wherein the compound includes RuOx, wherein the x is indicative of a desired number of atoms.

14. (Original) The semiconductor structure of claim 11, wherein the high temperature includes greater than about 750 degrees Celsius to less than about 801 degrees Celsius.

15. (Original) The semiconductor structure of claim 11, wherein the conductive layer passivates the insulator layer from undesired oxidation.

D7

16. (Currently Amended) A semiconductor structure for storing charges, comprising:
an insulator layer having a permittivity value; and

[redacted]

a single conductive layer abuttingly coupled to the insulator layer and adapted to mitigate diffusion, wherein the single conductive layer includes a compound and a substance, wherein the crystalline structure of the insulator layer describes a desired lattice plane such that the permittivity value of the insulator layer is greater than about 25.

D7

17. (Original) The semiconductor structure of claim 16, wherein the insulator layer includes ditantalum pentaoxide.

D8

18. (Original) The semiconductor structure of claim 16, wherein the conductive layer includes RuOx, wherein the x indicates a desired number of atoms.

19. (Original) The semiconductor structure of claim 16, wherein the desired lattice plane includes substantially a (001) plane.

20. (Original) The semiconductor structure of claim 16, wherein the desired lattice plane is described by three axes, wherein the desired lattice plane is parallel to two of the three axes and intersects one of the three axes.

D9

21. (Currently Amended) A capacitor comprising:

a first electrode;

a dielectric that includes ditantalum pentaoxide; and

a second single electrode having a compound that includes a first substance and a second substance, wherein the second single electrode also includes a trace amount of the first substance, wherein the compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion at a high temperature, wherein the compound includes RuOx, wherein the x is indicative of a desired number of atoms.

22. (Currently Amended) A capacitor comprising:

a first electrode;

a dielectric that includes ditantalum pentaoxide; and

a second single electrode having a compound that includes a first substance and a second substance, wherein the second single electrode also includes a trace amount of the first substance, wherein the morphology of the semiconductor structure remains stable when the trace amount of the first substance is oxidized during crystallization of the dielectric, wherein the compound includes RuOx, wherein the x is indicative of a desired number of atoms.

23. (Currently Amended) A capacitor comprising:

a first electrode;

a dielectric that includes ditantalum pentaoxide; and

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a second single electrode having a compound and a substance, wherein the crystalline structure of the dielectric describes a (001) lattice plane, wherein the compound includes RuOx, wherein the x is indicative of a desired number of atoms.

24. (Currently Amended) A capacitor comprising:

a first electrode;

a dielectric having a first compound that includes a first substance and a second substance, wherein the first compound includes ditantalum pentaoxide; and

a second single electrode having a second compound that includes a third substance and a fourth substance, wherein the second single electrode also includes a trace amount of the third substance, wherein the second compound in an as-deposited state includes a substantial amount of the fourth substance, wherein the trace amount of the third substance is oxidized during the crystallization of the dielectric such that a diffusion of at least one of the first substance and the second substance is inhibited, wherein the crystalline structure of the dielectric describes substantially a (001) lattice plane, and wherein the second compound includes RuOx, wherein the x is indicative of a desired number of atoms.

25. (Currently Amended) A capacitor comprising:

a first electrode having a substance that is selected from a group consisting of TiN, TiON, WNx, TaN, Ta, Pt, Pt-Rh, Pt-RhOx, Ru, RuOx, Ir, IrOx, Pt-Ru, Pt-RuOx, Pt-Ir, Pt-IrOx, SrRuO3, Au, Pd, Al, Mo, Ag, and Poly-Si;

a dielectric having a first compound that includes a first substance and a second substance, wherein the first compound includes ditantalum pentaoxide; and

a second single electrode having a second compound that includes a third substance and a fourth substance, wherein the second single electrode also includes a trace amount of the third substance, wherein the second compound in an as-deposited state includes a substantial amount of the fourth substance, wherein the trace amount of the third substance is oxidized during the crystallization of the dielectric such that a diffusion of at least one of the first substance and the second substance is inhibited, wherein the crystalline structure of the dielectric describes substantially a (001) lattice plane, and wherein the second compound includes RuOx, wherein the x is indicative of a desired number of atoms.

26-50. (Previously Canceled)

51. (Currently Amended) A memory device comprising:

an array of memory cells, wherein the array includes at least one capacitor that includes:

an insulator layer having a first compound that includes substances;

a single conductive layer having a second compound that includes a first substance and a second substance, wherein the single conductive layer also includes a trace amount of the first substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer;

an address decoder;

a row access circuitry;

a column access circuitry;

a controller; and

an input/output circuit.

52. (Currently Amended) An electronic system comprising:

a plurality of circuit modules includes a plurality of dies, wherein at least one die includes at least one array of memory cells, wherein the array comprises at least one capacitor that includes:

an insulator layer having a first compound that includes substances;

a single conductive layer having a second compound that includes a first substance and a second substance, wherein the single conductive layer also includes a trace amount of the first substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer;

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the single second conductive layer;

a plurality of leads coupled to the plurality of dies to provide unilateral or bilateral communication and control; and

a user interface.

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53. (Currently Amended) A computer system comprising:

a processor;

a memory system that comprises a plurality of memory modules, wherein one of the plurality of memory modules comprises a plurality of memory devices, wherein at least one memory device comprises at least one array of memory cells, wherein the array comprises at least one capacitor that includes:

an insulator layer having a first compound that includes substances;

a single conductive layer having a second compound that includes a first substance and a second substance, wherein the single conductive layer also includes a trace amount of the first substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer; and

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the single second conductive layer;

a plurality of command links coupled to the plurality of memory devices to communicate at least one command signal;

a plurality of data links coupled to the plurality of memory devices to communicate data;

a memory controller;

[redacted]

at least one user interface device, wherein the at least one user interface device includes a monitor;

at least one output device, wherein the at least one output device includes a printer; and

at least one bulk storage device.